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Independent Member

K C Mehta & Co LLP
Chartered Accountants

kcm Lens

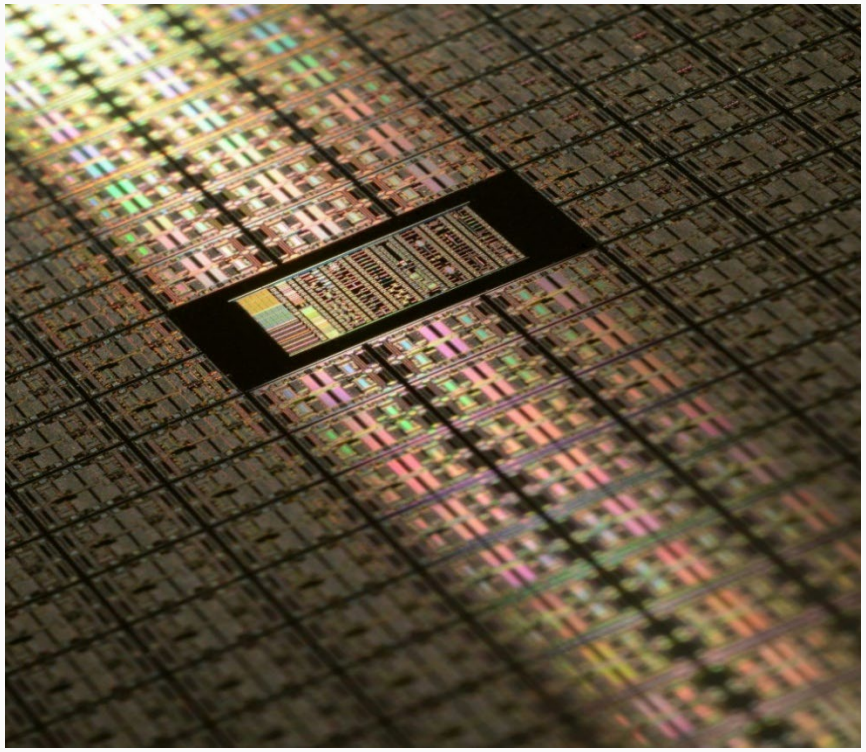
Chip Series – Volume 1

Meet the Semiconductors!
The Magic Inside Your Machines

January 2026

Introduction

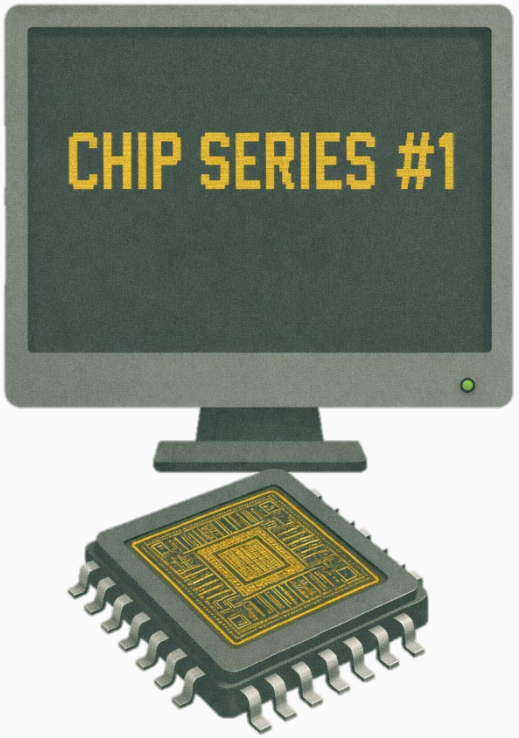
Introducing *kcm*Lens - a series of publication from KCM, offering sector specific. Under this series, we shall pick one sector, outline the value chain of that sector, and offer a deep dive analysis through the Lens of each segment of the value chain. This publication helps in developing a holistic understanding of the entire sector. The idea is to not only collate insights and updates on a particular sector for the readers, but to also present important takeaways from K C Mehta & Co LLP on that sector.



Following our recent series on EVs, we're back with a deep dive into the semiconductor industry. A Semiconductor or simply chip is a tiny piece of silicon that contains millions or even billions of microscopic electronic components like transistors and resistors. These chips acts as the "brains" of modern electronic devices.

The COVID-19 pandemic revealed critical semiconductor shortages, leading governments to classify chips as strategic assets. In this *kcm*Lens "Chip series" we will examine how the industry functions and what will be future outlook. This three-part series spans across full semiconductor value chain - Design (Vol I), Manufacturing & Fabrication (Vol II), and Assembly, Testing & Packaging (Vol III).

Volume I focuses on semiconductor design, covering the full design lifecycle, critical architectures and tools like EDA, IP, key innovations, global competitive landscape, and India's design ecosystem.

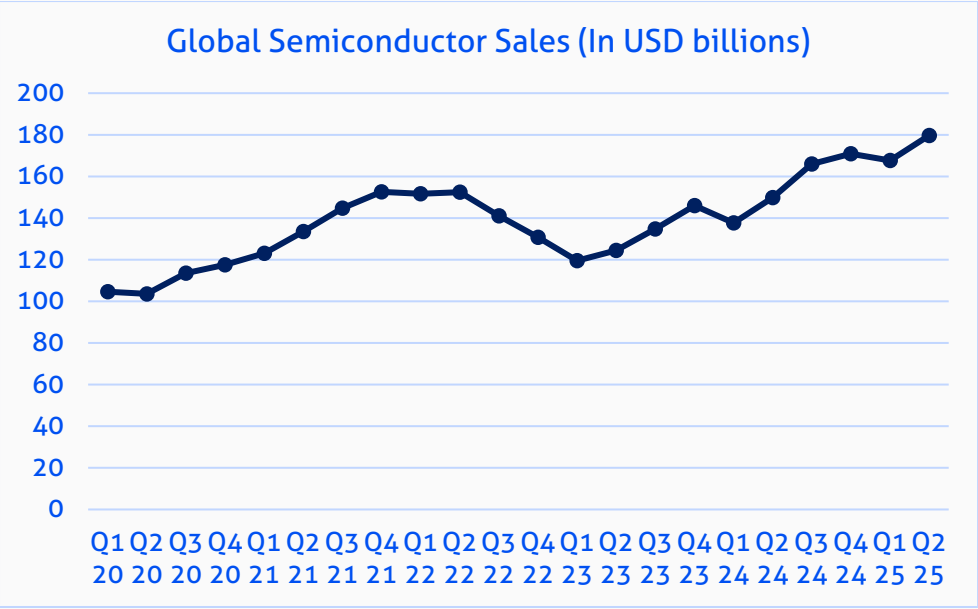


Content

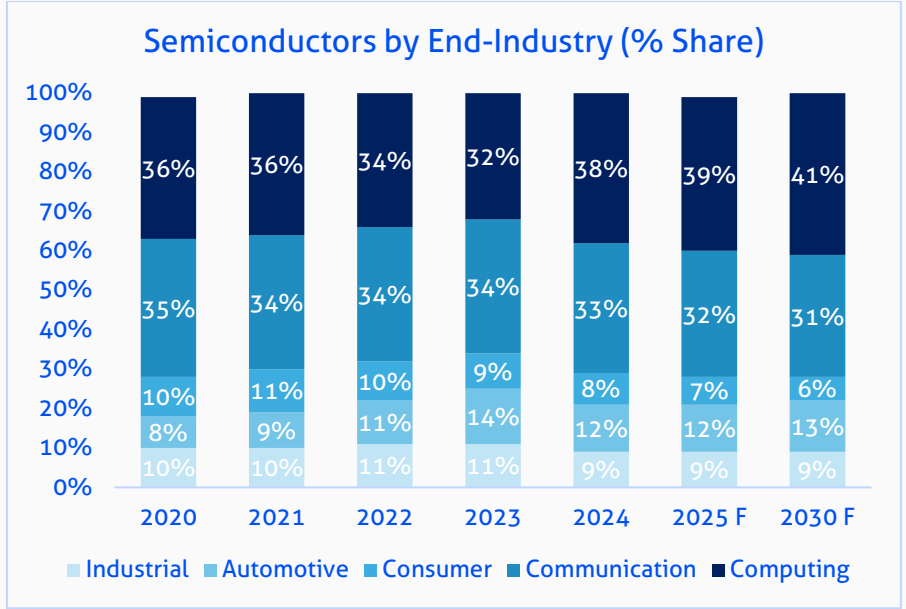
Silicon Goldrush: Betting on the Trillion-Dollar Decade

In 2024, global semiconductor revenues hit **US$627.6 billion - a 19.1%** increase year-over-year, largely driven by demand from AI, data-center spending, memory and advanced logic chips and the industry is on track to top roughly **US$700 billion in 2025**.

Analysts also expect the industry to **surpass US$1 trillion by 2030** as fabs, capacity expansion and capital expenditure scale up globally - manufacturers plan roughly **US$1 trillion of investment in new plants** through this decade to meet anticipated demand.



Source: Semiconductor Industry Association



Source: PwC

Semiconductor Family

Coverage

Semiconductor Family includes Analog Semiconductors and...

Based on their functions, semiconductor chips can be broadly classified in Analog and Digital.

Analog

Processes continuous signals like sound, light, or temperature to enable real-world interactions in electronics

Signal

Converts and conditions real-world continuous signals (voltage, current, radio waves) into digital form and vice versa

Example:

The chip that converts your voice to digital for calls; the radio front-end that connects your phone to Wi-Fi or LTE.

Power

Generates, controls and protects voltage rails; manages charging, power sequencing and efficiency across the system

Example:

The circuitry that lets your phone charge safely and extend battery life, the battery management in an electric car

Semiconductor Family

Coverage

...Digital Semiconductors

Digital

Processes binary logic (0s and 1s) to perform computation and storage tasks

Memory		Logic			
DRAM	NAND	CPUs	GPUs	ASICs	FPGAs
Volatile memory that stores data temporarily	Non-volatile memory that stores data persistently	Executes one task at a time	Handles many simple tasks at once	Custom designed for a single task	Customizable after manufacturing
Example: System RAM in laptops/phones	**Example:** SSDs and eMMC in laptops/phones; USB flash drives	**Example:** Application processor in a smartphone and PCs	**Example:** AI/Game rendering in consoles/PCs	**Example:** Used for specific use cases like car braking system, satellite chips	**Example:** Network packet processing in switches

System on a Chips (SoC)

Combines different chips into a single package for complete system functionality

Example:
Chips used in smartphone, smartwatch, streaming devices, IoT devices, Automotives

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Unveiling How Chips Power Every Industry

Coverage

Industry	Use Cases	Where used	Features	Semiconductor Type
Automotive	Engine & powertrain control ADAS & safety Infotainment & networking	ECUs, sensor hubs, radar/LiDAR modules, dashboards	Functional safety & reliability (ISO 26262)	MCUs/MPUs, power MOSFETs, SoCs, image sensors
Consumer Electronics	Smartphones & tablets TVs & set-top boxes Gaming consoles	Mainboards, display drivers, battery PMICs, SoCs	Power efficiency & cost	SoCs (application processors), DRAM/NAND, PMICs
Data Centres & HPC	Servers & storage arrays AI training/inference Networking	CPUs, GPUs, ASICs/TPUs, NICs, FPGAs	Compute throughput & energy efficiency	High-performance CPUs/GPUs, ASIC accelerators, HBM
Telecommunications	5G/6G base stations Core routers & switches Edge gateways	RF front-ends, line cards, optical modules	Bandwidth & latency	RF-ICs (GaN/GaAs), Ethernet PHYs, optical transceivers
Industrial & Automation	PLCs & motor drives Robotics & vision systems Smart sensors	Control cabinets, robotic arms, field sensors	Ruggedness & long lifecycle	Power semiconductors (IGBTs/MOSFETs), MCUs, sensor ICs
Aerospace & Defence	Avionics & flight controls Radar & EW systems	Flight computers, radar processors, transceivers	Radiation hardness & reliability	RAD-hard ASICs/FPGAs, mixed-signal ICs

Decoding the Semiconductor Ecosystem

Coverage

Tools needed at each step

Design	Manufacturing	Assembly, Testing and Packaging
EDA Tools for Designing Chip Semiconductor IP	Photolithography Deposition Etching Tools Ion Implantation tools	Dicing Machines Wire Bonders Encapsulation Testing Equipment

Fabless – Focused on designing chips only

NVIDIA, AMD, MEDIATEK, Qualcomm, BROADCOM, MARVELL

Foundry – Specialized in manufacturing chips at scale

tsmc, SAMSUNG, UMC, GlobalFoundries, Tower, SMIC

ATMP/OSAT – Specialized in Assembly, Testing and Packaging

ASE Technology Holding Co., Ltd., Amkor Technology, JCET, PTI Powertech Technology Inc., unisem, ChipMOS

Integrated Device Manufacturers (IDMs)

SAMSUNG, intel, ANALOG DEVICES, Micron, SK hynix, Texas Instruments

Chip Design - Tracing every step from concept to chip

Coverage

From Concept to Code: The Front-End Design Journey

Let's pull back the curtain on chip design and explore the **front-end process** where chip's functionality is defined and verified and **back-end process** steps where this logical design is turned into physical layout which can be manufactured.

Specification & Microarchitecture	RTL Coding (Logic Design)	Functional Simulation & Verification	Logic Synthesis	Static Timing Analysis (STA)
The design team refines the product spec into modules and Datapath and then partitions it into major blocks.	Engineers write synthesizable Verilog/VHDL for each block per your microarchitecture.	Simulate directed and random tests to hit coverage goals, apply formal model checking to prove critical protocols.	Use a synthesis tool to map RTL to gates under timing, power, and area constraints; then optimize to meet defined goals.	Perform STA across all PVT (process, voltage, temperature) to ensure all paths meet timing and fix discrepancies.

Real-World House Analogy for Chip Design

You define the requirement like area needed, number of rooms, utility needed (water, power, internet).	*Now in this step we will define these requirements in a language which builder will understand.*	*You put this specification into paper to see how the layout will look and modify anything if needed.*	*In this step you convert the design into specific material orders (beams, screws) and construction sequences.*	*In this step, you verify that the beams and columns can safely withstand all expected loads and potential*

Chip Design - Tracing every step from concept to chip

SSS

Coverage

Turning Code into Circuits: Back-End Design Process

Floorplanning	Placement	Clock Tree Synthesis (CTS)	Routing
Decide where the big blocks go (memory, connectors).	Put the small parts inside the plan so connections stay short.	Make sure the timing signal reaches every part evenly.	Draw the actual wires that connect everything.
Like deciding where bedrooms, kitchen, and garage sit on the plot.	*Like placing furniture so pathways are clear and efficient.*	*Like installing a reliable clock or timer system so lights turn on together.*	*Like running pipes and electrical wires through the walls.*

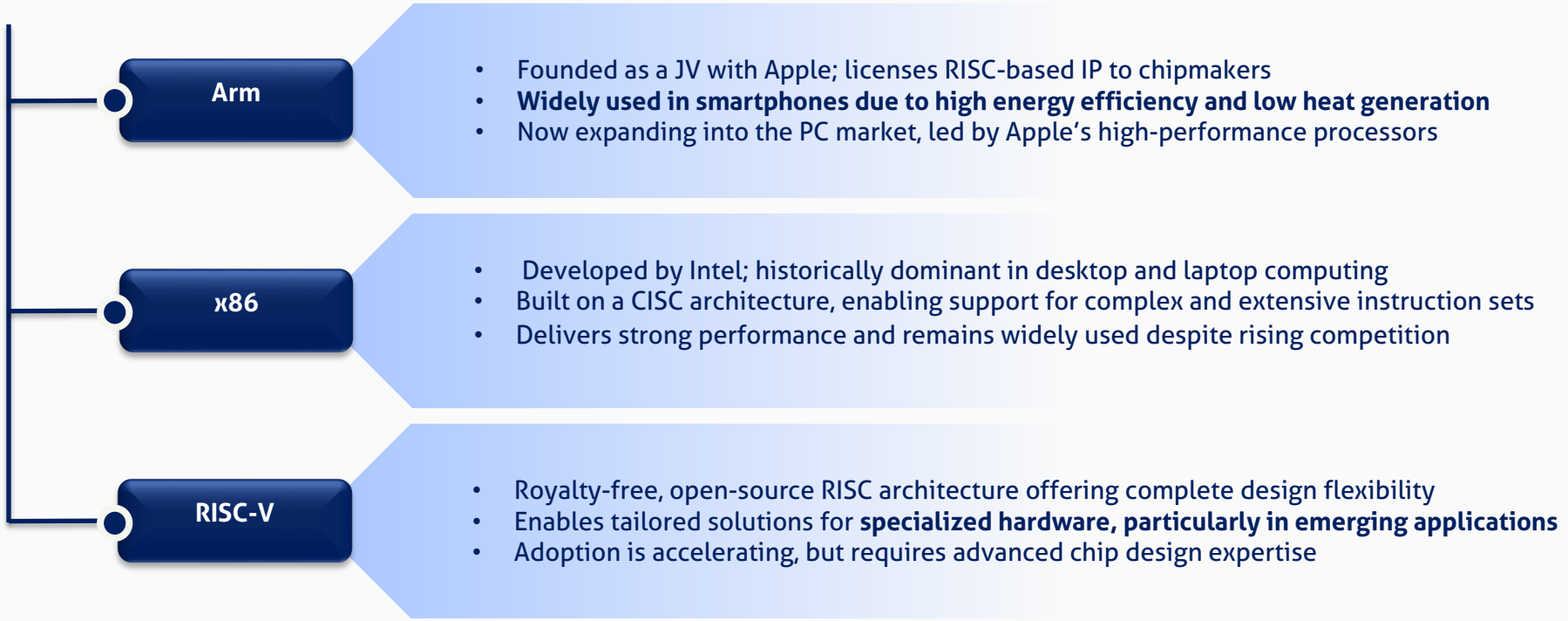
Mask Generation (GDSII/OASIS)	Timing Signoff	Physical Verification	Parasitic Extraction
Package the verified layout into the precise file format for foundry	Run final timing tests under many conditions and fix any deviations.	Run checks to ensure the layout follows manufacturing & design rule	Measure real effects of wires and metal layers (tiny resistances, delays).
Like delivering the final, permit-ready blueprints to the builder so construction can start	*Like testing that switches, pumps, & timers work under real conditions and fixing any that fail*	*Like verifying wall thickness, window spacing, & plumbing routes meet codes*	*Like measuring the real plumbing or electrical behavior, not just what was on the plan.*

Chip Design - Tracing every step from concept to chip

Coverage

The Blueprint Behind Every Chip, which is put to life by...

Chip architecture is the blueprint for a chip - how it's built and the "language" it uses to work. Different chips speak different languages, so software must match the chip. These differences affect speed, battery life, and what devices they're best for. Below are three common chip "languages"



But how do these complex architectures come to life on silicon? That's where Electronic Design Automation (EDA) tools step in — the invisible engine that turns chip blueprints into reality.

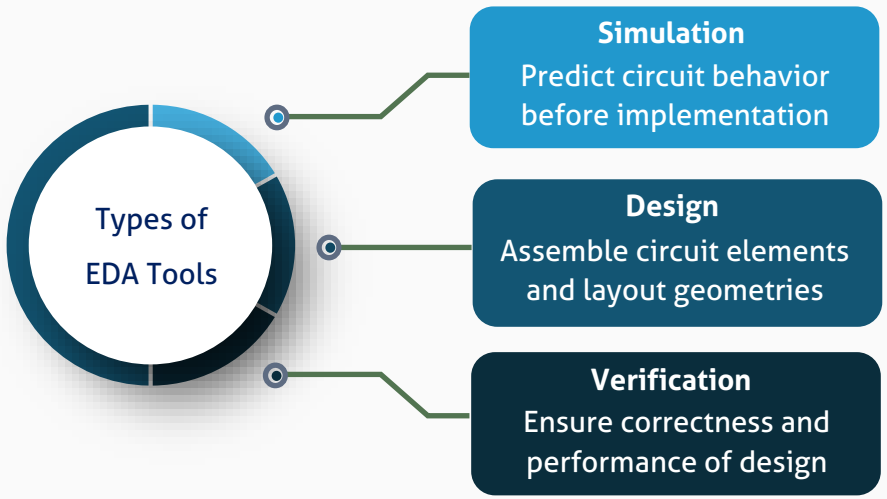
Chip Design - Tracing every step from concept to chip

Coverage

...Electronic Design Automation (EDA)

What are they and why are they important?

- EDA refers to specialized software that **provides virtual environment to design, verify, and test** integrated circuits (ICs) and systems-on-chip (SoCs).
- They make advanced chip design possible, cut errors and costs, and are essential for modern CPUs, GPUs, and AI chips which operate at nanometer level.



Market Concentration

The "Big Three" - **Synopsys, Cadence, and Siemens EDA** -which holds **more than 85% in 2023**, making EDA one of the most concentrated segments in semiconductor value chain.

SYNOPSYS® cadence SIEMENS

The concentration of advanced EDA tools among a few U.S. vendors has given the United States leverage to slow China's rise in chip design.

The U.S. tightened export controls on advanced EDA tools, forcing major vendors to restrict sales and support to China and disrupting access to cutting-edge design flows.

But China has also responded swiftly it has poured "Big Fund" capital into domestic EDA and equipment, accelerated local tool development and short-term workarounds (older tool versions, trials), and pushed long-term R&D and consolidation to reduce reliance on foreign suppliers.

EDA tools make chip design possible, but creating every component from scratch is time-consuming and expensive — this is where Semiconductor IP comes to rescue.

Chip Design - Tracing every step from concept to chip

Coverage

Semiconductor IP: The Ready-Made Building Blocks

Problem

As we saw in the earlier design process, creating a semiconductor chip from scratch is an intricate, multi-stage journey. Every stage requires specialized expertise, advanced tools, and multiple iterations to achieve the desired performance, power, and area targets.

For a new chip, this cycle can easily extend over **12 to 24 months or longer**, delaying the product's market entry and driving up development costs and in fast-moving industries such as consumer electronics, automotive, and AI accelerators, such delays in **time-to-market** can lead to loss in the market share.

Solution

A Semiconductor Intellectual Property (IP) block is a pre-designed, pre-verified, and reusable circuit or functional module that can be seamlessly integrated into a larger chip design.

In essence, it serves as a "ready-made building block" for a System-on-Chip (SoC), eliminating the need to design these components from the ground up.

Benefits

- Save development time by reusing proven designs,
- Reduce risk with pre-verified proven blocks,
- Accelerate time-to-market through faster integration
- Helps in creating differentiation by focusing engineering effort on the unique features

Leading Global Players

arm, cadence, SYNOPSYS, CEVA, Imagination, LATTICE SEMICONDUCTOR, Rambus

Leading Indian Players

MOSCHIP, Saankhya Labs, Silizium Circuits, eInfochips An Arrow Company, FASTSTREAM TECHNOLOGIES, MISTRAL ... Partners in Real Time, NETRASEMI Powering Intelligent Edge

Chip Design - Tracing every step from concept to chip

Measuring the success of Chip Design

Measuring the design metrics is crucial for assessing the performance, especially high the amount spent on R&D and considering how fast the technology is evolving. Now let's explore the key ratios commonly used in the industry to evaluate design efficiency, performance, and assess how one company

Time-to-Tape-Out

The duration from project start to final design handoff ("tape-out")

Average Design Cycle

Average time from concept to functional design completion over several projects

Tap-Out Success Rate

Percentage of first pass designs that are manufactured without major

Re-spins per project

Number of times a chip design had to be sent for another tape-out before working

Schedule Adherence

Measure how closely actual production follows the planned schedule

IP Reuse Ratio

Percentage of IP blocks reused from previous projects versus new

R&D Spend Ratio

How much of a company's revenue is being reinvested into research and

Next, we will see how the Moore's law affects chip technology and what it means to the performance of chips when Moore's law starts slowing.

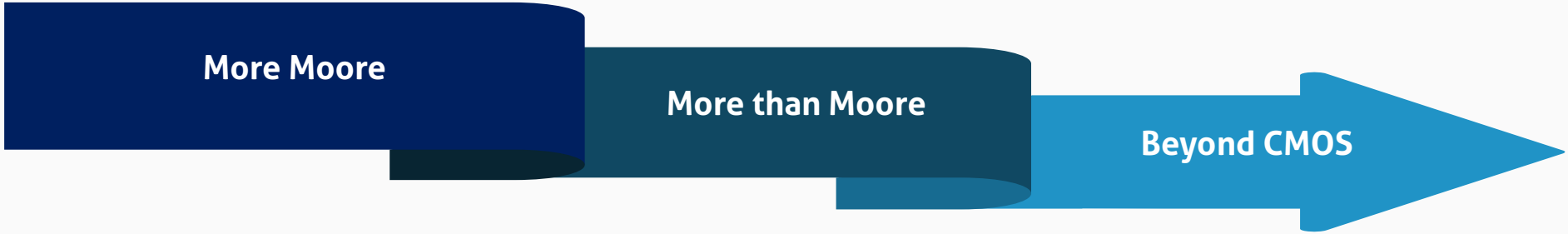
Chip Design - Tracing every step from concept to chip

Coverage

Moore's Law and the Future of Computing

Gordon Moore predicted in 1965 that the number of transistors on a chip would double approximately every 2 years, leading to rapid increases in **computing power**, **efficiency**, and **cost-effectiveness**.

For decades, progress followed Moore's Law - but as traditional scaling faces physical and economic limits, the industry is now advancing through three



What It Means:

Involves shrinking transistors to fit more on a chip, thereby increasing computational power and efficiency.

How It Works:

Smaller patterns via EUV lithography; using new transistor designs like Fin

What It Means:

Add new non-digital functions and components for better system integration.

How It Works:

Integrates functions like sensors, RF/analog, power circuits, and use 3D

What It Means:

Explore entirely new computing paradigms beyond traditional transistors.

How It Works:

Explores quantum computing, brain-inspired chips, spintronics, light-based

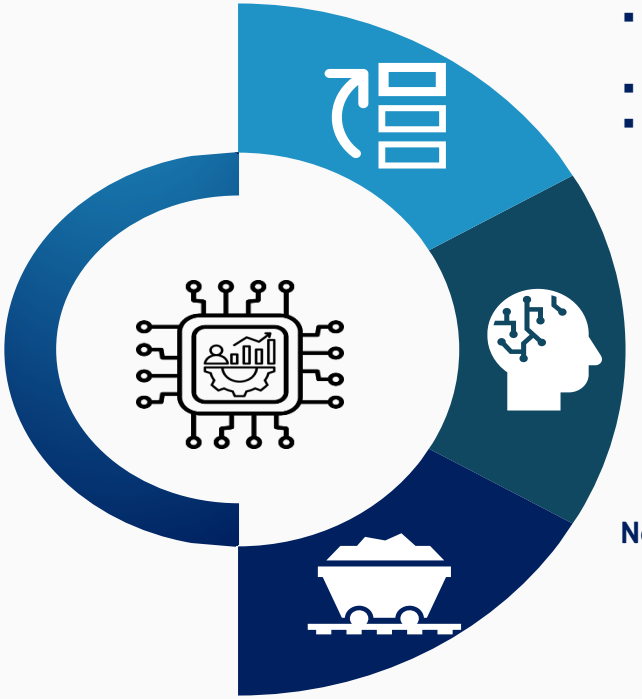
If Moore's Law is no longer the map, what's the new way forward? Let's chart the innovations beyond simple scaling.

Chip Design - Tracing every step from concept to chip

Coverage

Smarter, Smaller, Faster: The New Era of IC Design

Semiconductor chip design is rapidly evolving to meet the demands of next-gen computing. Innovations in architecture, automation, and materials are driving higher performance, energy efficiency, and design flexibility across industries.



3D Integration – Compact Design

- Vertical chip stacking improves bandwidth, lowers latency, and reduces power use.
- Enables efficient, high-density designs for AI and quantum computing.
- Reshaping chip design, demanding co-design to address layout, thermal, and interconnect challenges.

AI-Driven Chip Design

- AI enhances chip layout, defect detection, and design automation.
- Enables fast, cost-effective development of custom chips for edge, medical, and industrial use.
- Machine learning improves architecture quality and shortens design cycles.

Novel Materials

- SiC and GaN offer faster switching, higher power density, and compact design.
- These wide-bandgap semiconductors outperform silicon in high-speed, high-power applications and enables beyond silicon chips.

Our Take

By combining AI-assisted chip design with next-generation EDA tools, designing teams can produce faster, more power-efficient chips in less time offering a practical way to offset the slowing pace of Moore's law.

The Silicon Battleground

Coverage

Decoding Business Models in the Chip Industry

Fabless

Focus: Designing complete chips (SoC, ASIC, FPGA)
Manufacturing: Outsources fabrication
Revenue source: Selling finished silicon
Key Players:
Qualcomm, NVIDIA

IP Licensing & Royalty Model

Focus: Designing reusable IP blocks
Manufacturing: Handled by licensee (Not by IP provider)
Revenue source: License fees + royalties
Key Players:
SYNOPSYS, arm

Pure Design House

Focus: Designing custom chips
Manufacturing: Arranged by client or via partner foundry
Revenue source: Fixed price contracts
Key Players:
eInfochips An Arrow Company, wipro

Platform/Reference Design

Focus: providers sell a ready to use chip + system blueprint, Customer need to integrate at product level
Manufacturing: Handled by Client
Revenue source: From licensing/tools
Key Players:
Snapdragon, MEDIATEK

Open-Source Core Commercialization

Focus: Building commercial-grade, verified open-source cores
Manufacturing: Handled by client
Revenue source: Support, verification and specialization services, licensing
Key Players:
bluespec, SiFive

Joint Development

Focus: Co-design chips in partnership with large OEMs (e.g., Google, Amazon)
Manufacturing: Handled by Foundries
Revenue source: Milestone payments or shared product margins
Key Players:
BROADCOM, AMD

Our Take

In the near term, IP licensing and royalty streams are well positioned to benefit as chip designers prioritize faster time-to-market, generating steady, high-margin recurring revenue. At the same time, companies that provide AI infrastructure such as Nvidia, Google etc. are poised to gain as firms seek to tap the AI market and build more capable models.

The Silicon Battleground

Coverage

When Customer Becomes Competitor

Google, a big customer for NVIDIA's GPUs, launched its in-house designed chips

In late November 2025, a wave of reporting highlighted that Google's newest TPUs are beating Nvidia's flagship GPUs on some real world large-AI workloads - especially at price-performance for big model training and inference. There were two main reasons behind this wave of news.

The "Meta" Rumour	Several reports emerged that Meta, one of the biggest customers of Nvidia was in talks with Google to buy or lease TPUs for AI infrastructure.
Gemini 3's Success	Google announced that its latest AI model, Gemini 3, was trained exclusively on Google's TPUs. Its performance highlighted the significant scalability and efficiency advantages of TPUs.

Now let's evaluate the factors that contribute to the strengths of each chip.

	Purpose-built ASICs optimized for specific workloads, delivering high efficiency and throughput. Strong advantage in inference and large-scale deployments due to superior power efficiency and cost-
	General-purpose accelerators with exceptional raw computational power across diverse workloads. Highly versatile, allowing rapid adaptation to evolving AI architectures while maintaining strong performance.

Our Take

Google's TPUs are set to compete more aggressively with NVIDIA's GPUs as AI companies prioritize turning profitable using its cost-efficiency and operational efficiency. However, NVIDIA will remain strong due to GPUs' suitability for high-performance training workloads and the widespread adoption of CUDA, which makes shifting to Google's JAX/TensorFlow more challenging.

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Coverage

The U.S. still leads the race...

According to a 2022 study by the Semiconductor Industry Association and the Boston Consulting Group, U.S. based firms generated **46 percent of global semiconductor revenues in 2020 from design activities** alone.

Top 10 IC Design Houses in 2024

US: NVIDIA, Qualcomm, BROADCOM, MARVELL, MPS, AMD

Taiwan: MEDIATEK, REALTEK, NOVATEK

China: WILLSEMI 韦尔半导体

Reasons for US dominance

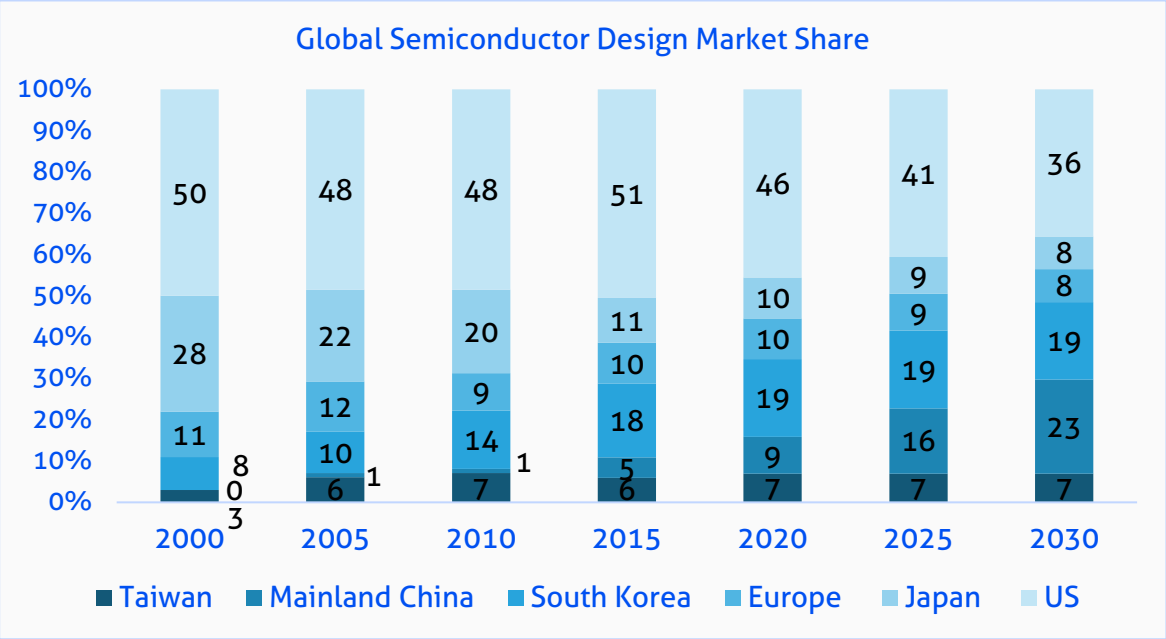
Robust R&D Investment	The U.S. chip firms reinvest heavily in R&D, driven by a virtuous cycle where sales leadership boosts profits, enabling further innovation
Comprehensive Ecosystem	The U.S. has leading fabless companies and supporting tools infrastructure like EDA (With Synopsys, Cadence, and Siemens EDA holding ~75% of the global market) providing a key competitive edge.
Talent Pipeline	It is home to world-class universities and tech hubs, cultivating a large pool of highly skilled engineers and designers who directly drive innovation and growth.
Government Support	Policies like the CHIPS and Science Act have directed substantial public funding toward advanced semiconductor research and workforce development

The Silicon Battleground

Coverage

...but China is closing the gap

While the U.S. maintains a strong position, its leadership faces challenges, particularly from China. A 2022 SIA–BCG study found the U.S. still leads the market, but China is catching up in legacy chips, though it remains behind in cutting-edge chips.



Source: Semiconductor Industry Association (SIA)-BCG Study

Our Take

China is rapidly closing design gaps but constraints in advanced tooling, high-end EDA/IP, and U.S./allied export controls mean the U.S. is likely to keep the lead for the next 15–20 years.

Factor for China's Emergence

1. Massive investment through National IC Strategy & Made in China 2025 with a goal to become self-sufficient and Global Leader in IC design and Manufacturing.
2. State-funded subsidies, tax breaks, land grants, and R&D credits allow Chinese chipmakers to operate at lower costs and sell products more cheaply than their rivals
3. China's chip design firms grew from 2,218 in 2020 to 3,626 in 2024. While many may not survive, still this growth underscores the rapid expansion of China's chip design industry
4. China mandates all domestic IoT chips adopt RISC-V by 2027, building an open-source ecosystem that bypasses Western licensing limits and drives innovation

The Silicon Battleground

Coverage

India's Chip Design Playbook

India has several companies - ranging from startups to established conglomerates and public institutions - that are actively involved in semiconductor chip design.

Indian Companies

TATA ELXSI, Bharat Electronics, L&T Technology Services, MosChip, Sankalp Semiconductor (An HCLTech Company), Mistral (... Partners in Real Time), Aura Semiconductor, CDIL Semiconductors, Fermionic, Aheesa Digital Innovations, SensesEmi, WiSig Networks, Mindgrove, Saankhya Labs, AGNIT, Morphing Machines, eInfochips (An Arrow Company), NetraSemi (Powering Intelligent Edge), Incore Semiconductors, Blueberry

India's major Chips and their use cases

Chip Type	Target Industries & Use-Cases
Microcontrollers & SoCs	IoT devices, edge computing, space/defence applications
Analog / Mixed-Signal / RF / MEMS	Telecommunications, IoT, consumer electronics, industrial sectors
Display & Compound Semiconductors	Mobile devices, laptops, automotive displays, medical & defence systems
Power Electronics (IGBTs/MOSFETs)	Electric vehicles (two/four-wheelers), solar energy, industrial automation
ASICs & Custom VLSI IP	Avionics, industrial control systems, telecommunications, embedded systems

The Silicon Battleground

Coverage

Silicon Sunrise: India's Chip Design Moment

The Government of India has made semiconductor design a strategic priority to position the country as a global tech hub. The industry, valued at **$45–50 bn in 2024-25**, is projected to reach **$100–110 bn in 2030**, supported by comprehensive policies to drive growth. Key initiatives include:

Policy Framework

India Semiconductor Mission (ISM) with outlay of 72,000 cr to develop the semiconductor ecosystem
Partnership with various countries like **India-U.S. Initiative on Critical and Emerging Technology**

Financial Support

Design Linked Incentive which will reimburse 50% of eligible design cost (capped at ₹15 cr.)
Deployment linked incentive with incentive of 4-6% of net sales (capped at ₹30 cr.)

Infrastructure Development

Selected **72 startup for the EDA tools support** under the Chip Design Infrastructure Support
Through **ChipIN centers provided EDA tools access to 85,000 B.Tech, M.Tech and PhD** level students

Workforce Development

Introduced **AICTE curriculum for VLSI Design & IC manufacturing Centers of Excellence (CoE) and ChipIN centers** to give the hands-on experience and prepare a skilled workforce

Our Take

India contributes about **20% of the world's semiconductor design engineers** but holds only a small share of global chip-design output and IP. While the government **initially prioritized fabs and OSAT, greater policy support is now needed for the domestic design ecosystem**. Strong domestic chip design can create a steady pipeline of IPs, shorten development cycles, reduce dependence on foreign suppliers, and insulate the supply chain from export controls and geopolitical shocks. To build a robust semiconductor ecosystem, design is an essential part of the value chain.

The Silicon Battleground

After having built the architecture and verified it in the lab, the next and equally critical step is turning that design into manufacturable silicon. Turning blueprint into silicon is a distinct industry and it comes with its own challenges, risks and competitive rules.

Let's look at the reason why:

Design = Innovation & IP	Designing focus on architectures, RTL, verification, EDA tools, and differentiation through features.
Manufacturing = Industrialization & Scale	Manufacturing focus on process technology, yield, capital intensity, supply chain and massive operational discipline.
Different economics & players	Design is talent-driven, while manufacturing is capital-intensive, scale-driven, and often concentrated in countries creating distinct risks and approachs.
Different risks & KPIs	For designers, the key metrics are time-to-market and tape-out success; for fabs, they are yield, throughput, cost per wafer, and equipment uptime.

In the Chip Series #2, we will explore how completed chip designs are manufactured from silicon - fabrication processes and the tools and equipment that enable them, outline the principal business models that govern fabrication and supply, and analyze the competitive landscape to identify the companies and regional ecosystems that lead semiconductor manufacturing today.

Coverage

Abbreviations

Abbreviation	Meaning
DRAM	Dynamic Random Access Memory
ASIC	Application Specific Integrated Circuits
FPGA	Field Programmable Gate Array
ADAS	Advanced Driver Assistance Systems
ECU	Engine Control Unit
LiDAR	Light Detection and Ranging
MCUs	Microcontrollers
MPUs	Micro Processing Units
MOSFETs	Metal-Oxide-Semiconductor Field-Effect Transistor
PMICs	Power Management Integrated Circuits
TPUs	Tensor Processing Unit
NICs	Network Interface Card
HBM	High Bandwidth Memory
RF-ICs	Radio Frequency Integrated Circuits
ATMP	Assembly, Testing, Marking and Packaging
OSAT	Outsourced Assembly and Testing
RTL	Register-Transfer Level

Abbreviation	Meaning
VHDL	Very High-Speed Integrated Circuit Hardware Description Language
GDSII	Graphic Data System II
OASIS	Open Artwork System Interchange Standard
CISC	Complex Instruction Set Computer
RISC-V	Reduced Instruction Set Computer Generation 5
EUV Lithography	EUV Lithography - Extreme Ultraviolet Lithography
FETs	Field Effect Transistor
GAAs	Gallium Arsenide
CMOS	Complementary Metal-Oxide-Semiconductor
SiC	Silicon Carbide
GaN	Gallium Nitride
CUDA	Compute Unified Device Architecture, NVIDIA's parallel computing platform
CHIPS Act	Creating Helpful Incentives to Produce Semiconductors Act
RF	Radio Frequency
MEMS	Micro-Electro-Mechanical Systems

About kcmLens

kcmLens is a special publication prepared by the Strategic Advisory team at K C Mehta & Co LLP. This publication is intended to provide deep dive into the value chain of a particular industry. The idea is to provide the reader an end-to-end understanding of a particular industry through the Lens of each segment of the value chain of that industry. This would act as a ready reference for professionals, who seek to understand their client's business and as an update document for business leaders for tracking recent developments in their industry.

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